What is claimed is:

(Claim 1) 1. A filter circuit processing an input signal, said filter circuit comprising:

an operational amplifier containing an input terminal and an output terminal, said input signal being received on said input terminal;
a passive element coupled between said input terminal and said output terminal;
a first capacitor and a first resistor connected in series, and providing said input signal to said input terminal; and
a second resistor connected in parallel to said first capacitor and said first resistor connected in series.

(Claim 2) 2. The filter circuit of claim 1, wherein said second resistor has more resistance than said first resistor.

(Claim 3) 3. The filter circuit of claim 2, wherein said passive element comprises a resistor.

(Claim 4) 4. The filter circuit of claim 2, wherein said passive element comprises a capacitor.

(Claim 5) 5. A phase locked loop (PLL) generating an output signal synchronized with a reference signal, said PLL comprising:

a phase frequency divider (PFD) comparing the phase of said output signal with the phase of said reference signal and generating an error signal representing the difference of phases of said output signal and said reference signal;
an active filter circuit generating a correction signal based on a magnitude of said error signal, said active filter circuit comprising:
an operational amplifier containing an input terminal and an output terminal;
a passive element coupled between said input terminal and said output terminal;
a first capacitor and a first resistor connected in series, and providing said error signal as an input signal to said input terminal; and
a second resistor connected in parallel to said first capacitor and said first resistor connected in series; and
an oscillator adjusting the phase of said output signal according to said correction signal.

(Claim 6) 6. The PLL of claim 5, wherein said second resistor has more resistance than said first resistor.

(Claim 7) 7. The PLL of claim 6, wherein said passive element comprises a resistor.

(Claim 8) 8. The PLL of claim 6, wherein said passive element comprises a capacitor.

(Claim 9) 9. The PLL of claim 8, further comprises:

a charge pump converting said error signal into said input signal; and
a feedback divider dividing said output signal to generate a signal for comparison by said PFD,
wherein said oscillator comprises a voltage controlled oscillator.

(Claim 10) 10. A device comprising:

a filter circuit processing an input signal, said filter circuit comprising:
an operational amplifier containing an input terminal and an output terminal, said input signal being received on said input terminal;
a passive element coupled between said input terminal and said output terminal;
a first capacitor and a first resistor connected in series, and providing said input signal to said input terminal; and

a second resistor connected in parallel to said first capacitor and said first resistor connected in series.

(Claim 11) 11. The device of claim 10, further comprising a processing unit processing a plurality of digital values generated using an output signal received on said output terminal.

(Claim 12) 12. The device of claim 11, further comprising:

a phase locked loop (PLL), said PLL comprising said filter, and an oscillator being controlled by said output signal, said PLL generating a clock signal; and

an ADC sampling an analog signal at time points specified by said clock signal to generate said plurality of digital values.

(Claim 13) 13. The device of claim 11, wherein said second resistor has more resistance than said first resistor.

(Claim 14) 14. The device of claim 13, wherein said passive element comprises a resistor.

(Claim 15) 15. The device of claim 13, wherein said passive element comprises a capacitor.